SYSTEM AND METHOD FOR REDUCING THE EFFECTS OF CLOCK HARMONIC FREQUENCIES

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention generally relates to wireless communications and, more particularly, to a system and method for reducing the effects of clock generated harmonics in the transceiver passband of a wireless communications device.

2. Description of the Related Art

Processors, such as microprocessors, are an integral part of many electronic products, including a typical wireless communications device. Microprocessors are typically used to execute instruction sets and to generally control the operation of devices. A clock is used with the typical microprocessor to provide a frequency at which the microprocessor operates. A crystal is a conventional and inexpensive way of supplying a microprocessor reference frequency. As is well known, spurious frequencies such as harmonics, are generated by the clock, along with the desired clock frequency. These spurious frequencies, as well as the crystal resonant frequency, "leak" through to other circuits on the device printed circuit board through conductance on the power lines or grounds, and through radiation. These spurious frequencies can interfere with the operation of a device by manifesting themselves as noise to other portions of the wireless communications device..

A wireless communication device transceiver circuit is especially susceptible to interference from spurious signals. In some instances, the spurious signals have frequencies equal to the carrier

frequency of the wireless communications device. By equal to the carrier frequency, it is to be understood that this includes spurious signals that have some power in the passband of the wireless communication device. These spurious signals may provide undesirable noise and degrade

5   performance of the device. For example, noise in the passband of a receiver can degrade sensitivity, while noise in a transmitter passband can violate system specifications, or raise the general noise floor of the system in which the wireless device is operating.

To solve spurious signal and interference problems, it is

10   typically necessary to add filtering circuits or shielding to the circuit board. However, this solution takes time and adds to the total parts count. In some instances, the size and position of the board may limit the filtering that can be provided. It is known to change the clock frequency to avoid harmonic interference with the local oscillator or other

15   transceiver circuitry. However, it is not desirable to reselect wireless device crystals to accommodate printed circuit board filtering issues. In wireless devices that operate with more than one transceiver frequency, it may be difficult to find a single clock frequency that supports the operation of the digital circuitry, and yet avoids interfering with at least

20   one of the transceiver frequencies.

It would be advantageous if the undesirable effects of spurious frequencies, such as those harmonically related to a clock, could be eliminated from or substantially reduced in the passband of a transceiver without special filtering.

25   It would be advantageous if a wireless communications device could be operated at a plurality of transceiver frequencies while

reducing the noise effects of spurious signals related to clock generated harmonics.

SUMMARY OF THE INVENTION

5   The present invention was created to address the problem of reducing the effects of clock-generated harmonics in the transceiver passband of a wireless communications device. The invention recognizes that the harmonics generated by a clock can leak through to the transceiver and cause sensitivity, noise, and system specifications

10   problems in the wireless device. The invention also recognizes that the avoidance of harmonics by the use of filtering circuits or shielding, or by changing crystals is not always desirable or effective. The invention addresses the above-mentioned problem by selectively adjusting clock frequencies so that the harmonics associated with the selected clock

15   frequency do not substantially interfere with the operating passband of the transceiver.

          Accordingly, a system is provided for reducing the effects of spurious frequencies that substantially interfere with the performance of a wireless communications device. The system comprises a processor

20   having a clock frequency input and a clock having an output connected to the processor input to supply the clock frequency. The clock frequency is the frequency at which the processor operates. The clock has an input for selecting a clock frequency to provide to the processor.

          The system also includes a transceiver supplying a plurality

25   of selectable communications passbands. If the wireless communications device is a telephone for example, the transceiver frequency (passband)

changes as a function of the mode in which the phone is operating (advanced mobile phone service (AMPS), personal communication services (PCS), global system for mobile communications (GSM), code division multiple access (CDMA), or wideband CDMA (W-CDMA)). In response to changing operating modes, the clock adjusts the clock frequency. The clock frequency is selected so that harmonic frequencies associated with the clock frequency do not substantially interfere with the transceiver passband.

Additional details of the above-described system and a method for reducing the effects of spurious frequencies in a wireless device are presented below.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic block diagram depicting the system for reducing the effects of spurious frequencies in a wireless communications device in accordance with the present invention.

Fig. 2 is a flowchart illustrating the method for reducing the effects of spurious frequencies in a wireless communications device in accordance with the present invention.

Fig. 3 is a flowchart illustrating the method for avoiding spurious frequencies in the transceiver passband of a wireless communications device in accordance with the present invention.

Fig. 4 is a flowchart illustrating the method for reducing the effects of clock harmonics in the passband of a wireless communications device in accordance with the present invention.

Fig. 5 is a flowchart illustrating another aspect of the method for reducing the effects of clock harmonics in the passband of a wireless communications device in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

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Fig. 1 is a schematic block diagram depicting the system 100 for reducing the effects of spurious frequencies in a wireless communications device 102 in accordance with the present invention. The

10   device 102 includes a microprocessor 104 with an input on line 106 to accept a clock frequency. A clock 108 has an output on line 106 to supply a clock frequency to the microprocessor 104. This clock frequency is often the fundamental frequency of a crystal source. The clock 108 is capable of providing a plurality of predetermined clock frequencies, as described

15   below.

It will be appreciated that other types of processors and designs may be substituted for the microprocessor and clock. For example, a processor and a clock may be provided on an application specific integrated circuit as a single component. Also, other types of

20   processors, such as gate arrays or other programmable logic devices may be used.

A transceiver 110 has a port to transmit and receive a carrier frequency via an airlink interface. The airlink interface is represented by antenna 112. The transceiver 110 may include de/modulating circuits,

25   power amplifiers, receivers, frequency sources, and other components (not shown), but well known in the art. The transceiver is typically a

multiband transceiver having an input on line 114 for accepting commands selecting one of a plurality of communication passbands. Alternately but not shown, the device 102 includes a plurality of transceivers, each tuned to operate in a different passband.

5   Harmonics are generated by the clock 108, along with the desired clock frequency needed to operate the microprocessor 104. Harmonics are signals that are at harmonic frequencies. Harmonic frequencies are multiples of another frequency or frequencies called the fundamental frequency or frequencies. Generally, harmonic frequencies

10   may be any ratio of integers multiplied by the fundamental frequency or some combination of the fundamental frequencies. Harmonics are typically numbered in increasing order of the ratio. In one common scheme for naming harmonics, the denominator in the ratio is one. The first harmonic frequency is equal to the fundamental frequency. The

15   second harmonic frequency is equal to two times the fundamental frequency, and, for example, the 46th harmonic frequency is equal to 46 times the fundamental frequency. This common scheme for naming harmonics is used in this patent. It is to be understood, however, that the methods and devices described herein can be similarly used with

20   harmonic frequencies that are non-integer multiples of the fundamental frequency.

These harmonics can appear as spurious frequencies that can radiate or conduct into the transceiver 110, interfering with the carrier frequencies. The radiation or conduction of these spurious frequencies are

25   represented by the dashed line with the reference designator 116. Although the harmonics can be filtered or shielded from the transceiver

110, this problem is often more directly solved by selecting a crystal

frequency with harmonics that avoid the transceiver passband. However,

selecting a crystal frequency that generates harmonics outside the

transceiver passband can become difficult, or even impossible, if the

5   device 102 has multiple transceivers or if the transceiver 110 is expected

to operate at more than one carrier frequency (as shown).

To this end, the microprocessor 104 operates at more than

one clock frequency. The clock 108 has an input on line 118 to accept

selections for clock frequencies, and supplies clock frequencies in response

10   to the selections on line 118. In some aspects of the system 100, different

clock frequency can be selected by selecting between one or more different

crystals oscillating at different frequencies. In other aspects of the system

100, different clock frequencies can be selected by tuning a phase lock loop

to a different frequency.

15   The following example illustrates the operation of the

present system 100. When the wireless device 102 is operating in a first

mode, such as code division multiple access (CDMA), the clock 108

provides a first reference frequency to the microprocessor 104. In turn,

the transceiver 110 operates in the CDMA passband of approximately

20   1900 megahertz (MHz). The CDMA passband is selected in response to

commands on line 114. When the wireless device 102 switches to a second

mode, such as the AMPS (analog) mode, in response to commands on line

114, the transceiver 110 switches passband frequencies. The AMPS

center frequency is approximately 900 MHz.

25   If the first clock frequency generated by clock 108 has an

associated harmonic that occurs at 900 MHz, the transceiver signals may

be degraded when the transceiver 110 switches to the AMPS mode. To avoid such interference, a second clock frequency is selected using the clock 108 input on line 118. In response, the clock 108 provides the second clock frequency to the microprocessor 104 on line 106. The second clock

5   frequency is predetermined so that the harmonics associated with it do not interfere with the second mode (AMPS) passband.

More specifically, if the first clock frequency is 19.2 MHz, the 46th harmonic is 883.2 MHz. This is a frequency that does not interfere with the CDMA passband centered around 1900 MHz. However, the 46th

10 harmonic does interfere with the transceiver 110 when switched into the AMPS mode at approximately 900 MHz. To solve the interference problem, the second clock frequency is selected to be 26.24 MHz. The 46th harmonic at 1207 MHz is far removed from the AMPS passband.

Fig. 2 is a flowchart illustrating the method for reducing the

15 effects of spurious frequencies in a wireless communications device in accordance with the present invention. Although the method (and the other methods described below) is depicted as a sequence of numbered steps for clarity, no order should be inferred from the numbering unless explicitly stated. It should be understood that some of these steps may be

20 skipped, performed in parallel, or performed without the requirement of maintaining a strict order of sequence. The method starts at Step 200. Step 202 provides a plurality of selectable passband ranges for the wireless communications device. Step 204 selects one of the passband frequency ranges. Step 206 determines a clock frequency that produces no

25 substantial spurious signals (spurs) in the selected passband frequency range. Step 208 adjusts a clock to generate a clock signal at the clock

frequency. Step 210 drives a processor with the clock signal. In one aspect of the invention, selecting one of the passband frequency ranges in Step 204 includes providing a cellular passband frequency range and a PCS passband frequency range.

5   Fig. 3 is a flowchart illustrating the method for avoiding spurious frequencies in the transceiver passband of a wireless communications device in accordance with the present invention. The method starts at Step 300. Step 302 generates a clock frequency with harmonics at a first frequency. Step 304 generates a transceiver carrier

10   at a second frequency. Step 306 selects the clock frequency so that the first frequency does not equal the second frequency.

In some aspects of the method, generating a transceiver carrier at a second frequency in Step 304 includes generating a transceiver carrier with a center frequency of approximately 900 MHz. A

15   further step, Step 301, initially generates a clock frequency at 19.2 megahertz (MHz) with a 46th harmonic at 883.2 MHz. Then, selecting the clock frequency so that the first frequency does not equal the second frequency in Step 306 includes increasing the clock frequency from 19.2 MHz to 26.24 MHz.

20   Fig. 4 is a flowchart illustrating the method for reducing the effects of clock harmonics in the passband of a wireless communications device in accordance with the present invention. The method starts at Step 400. Step 402 generates a clock frequency with harmonics at a first frequency. Step 404 generates a transceiver carrier at a second frequency.

25   Step 406 changes the clock frequency so that the first frequency does not equal the second frequency.

Fig. 5 is a flowchart illustrating another aspect of the method for reducing the effects of clock harmonics in the passband of a wireless communications device in accordance with the present invention. The method starts at Step 500. Step 502 generates a clock frequency with harmonics at a first frequency. Step 504 generates a transceiver carrier at a second frequency not equal to the first frequency. Step 506 changes the transceiver carrier to the first frequency. Step 508 changes the clock frequency to a clock frequency with harmonics at a third frequency, not equal to the first frequency.

A system and a method are provided for reducing the effects of spurious frequencies in the transceiver passband of a wireless communications device. Examples of the invention have featured specific reference frequencies, passband frequencies, and modes of operation, however, it should be understood that the present invention is not limited to any particular frequencies or modes of operation. Examples have also been given of a wireless telephone device, however, it should be understood that the invention is applicable to a broader field of wireless operations. Other variations and embodiments of the invention will occur to those skilled in the art.